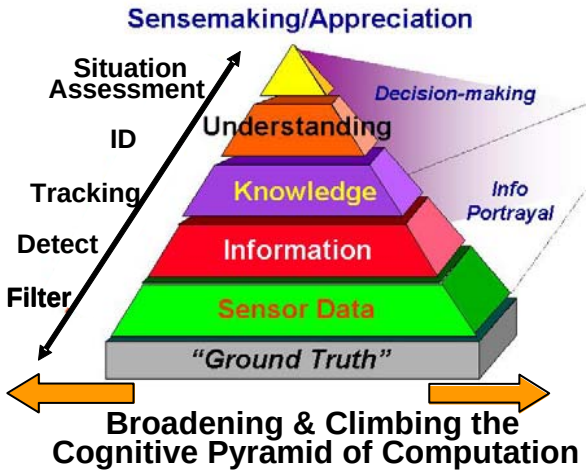
Amending Moore's Law for Embedded Applications

29 Sep 2004



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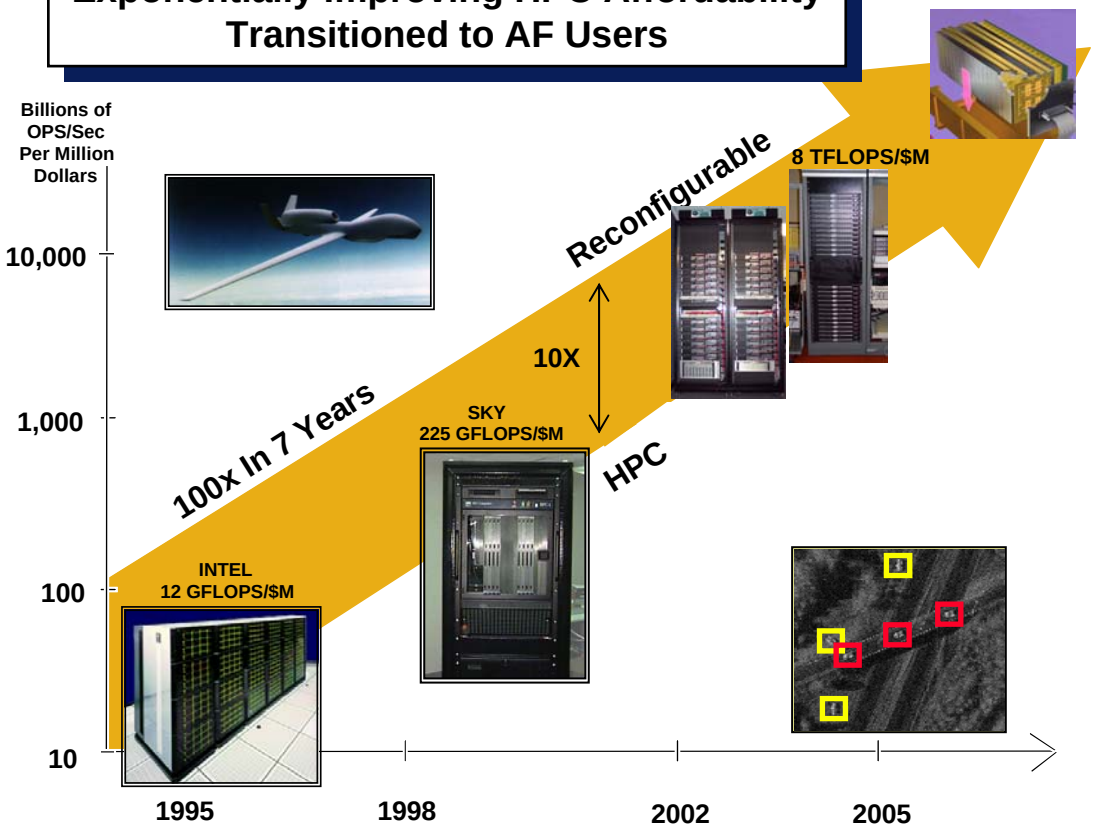
Contribution of Moore's Law to Improvements of Embedded Systems

- **Price/Performance:** Gigaflops/$M affordability
- **Memory Capacity:** programming simplifications
- **Steep memory hierarchy:** programming inefficiencies and complexities
- **New flexibilities:** e.g. reconfigurable hardware
- **New complexities:** software and parallelism
- **Dramatic new system capabilities**

Extending the Affordability Trend

Exponentially Improving HPC Affordability Transitioned to AF Users



Projection:
2007: 60 trillion flops/$M
2010: 360 trillion flops/$M

CHALLENGE:

Develop and Incorporate the Most Affordable Embedded Information Technology Available

APPROACH:

- Leverage Commercial Investments In Computer Architectures
- Develop Portable Embedded DoD Applications using middleware standards
- Leverage DARPA, and Other DoD Efforts In Emerging Architectures

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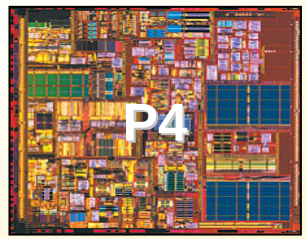
Airborne COTS HPC

25 Dual-Xeon Compute Nodes

- **Dual GbE Network (80 MB/s per link)**
- **1U Rack-mounted**
- **$87K approximate cost -** 3.1 DP TFLOPS/$1M

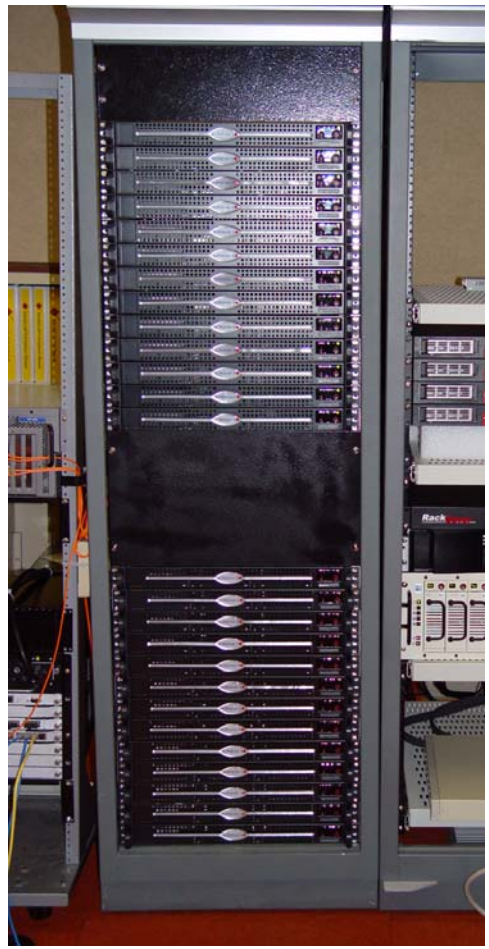
Commodity Compute Node:

- **Dual 2.66 GHz Intel Pentium 4 Xeon CPU**
  - **512KB L2 Cache**
  - 21.3 SP GFLOPS **peak per node**
- **Dual GbE network interfaces**
- **6 GB DDR SDRAM**



Peak Performance:

- **532.5 GFLOPS** (IEEE 32 bit)



Swathbuckler Cluster

(Coyote)

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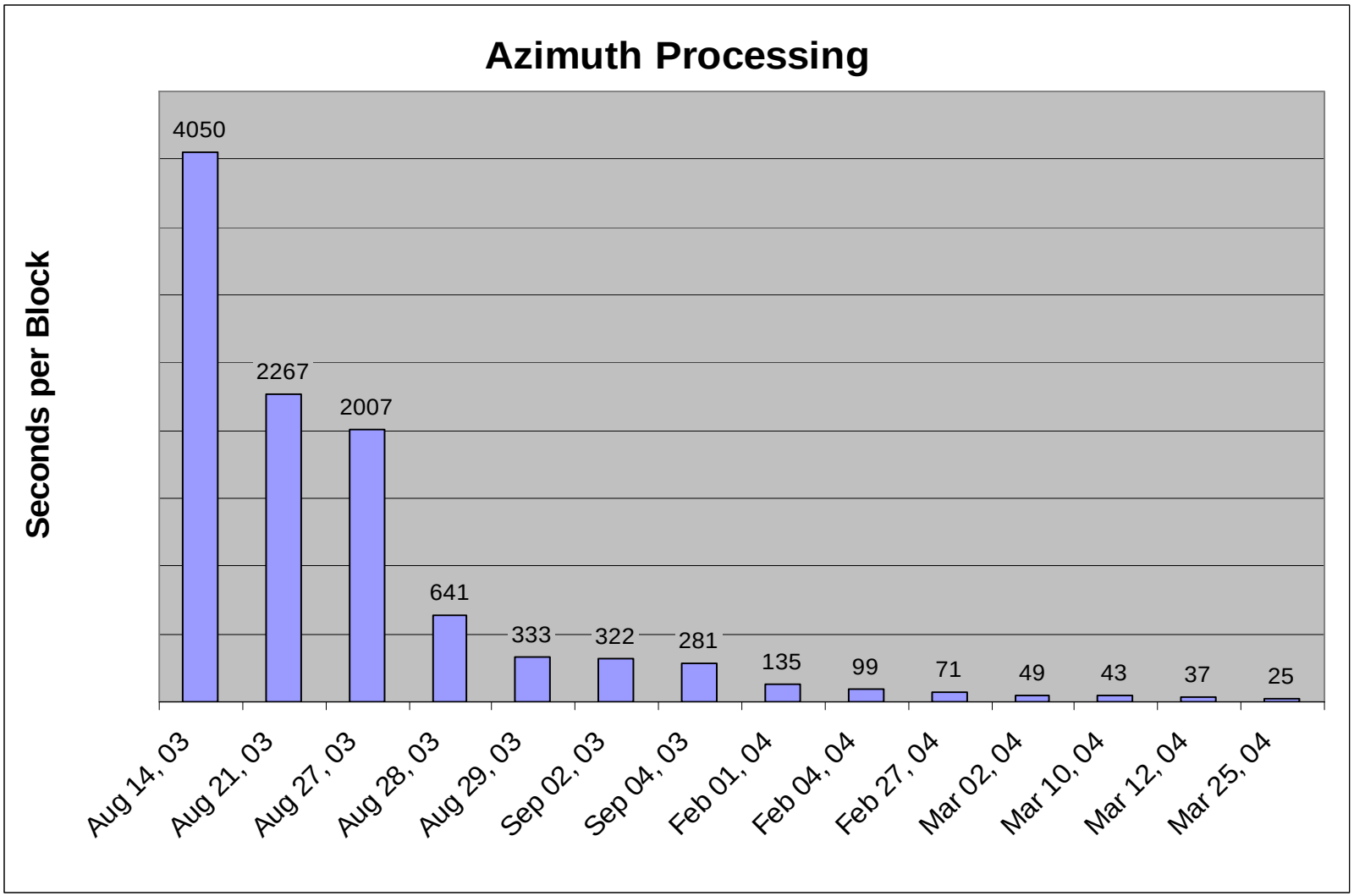
Can we preserve historical improvement rates?



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Heterogeneous HPC Hardware

- 48 Nodes in 2 cabinets
- Server product leverage
- Each node with: Dual 2.2 GHz+ Processors
  - 4 Gbyte SDRAM
  - Myrinet 320 MB/sec Interconnect
  - 80 GB disk
  - 12 M gate Adaptive Computing Board
- 34 TOPs demonstrated
- Online FEB 2003 supporting HIE, TTCP and SBR projects

Heterogeneous High Performance Computer

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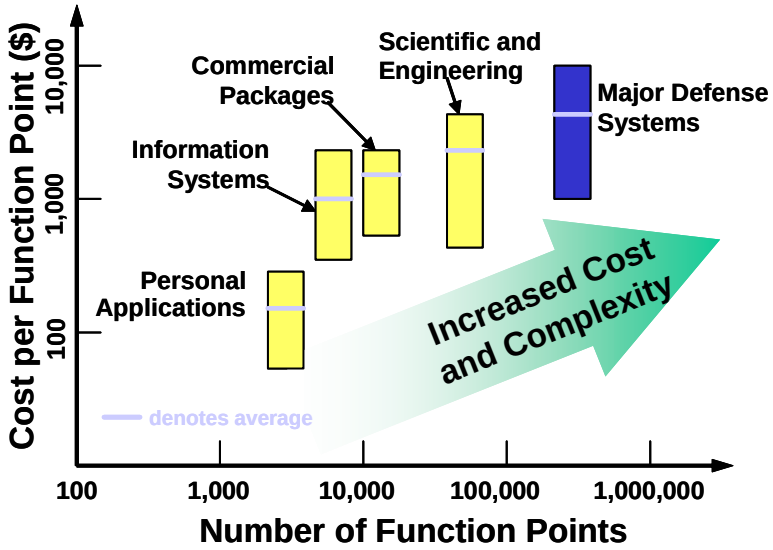
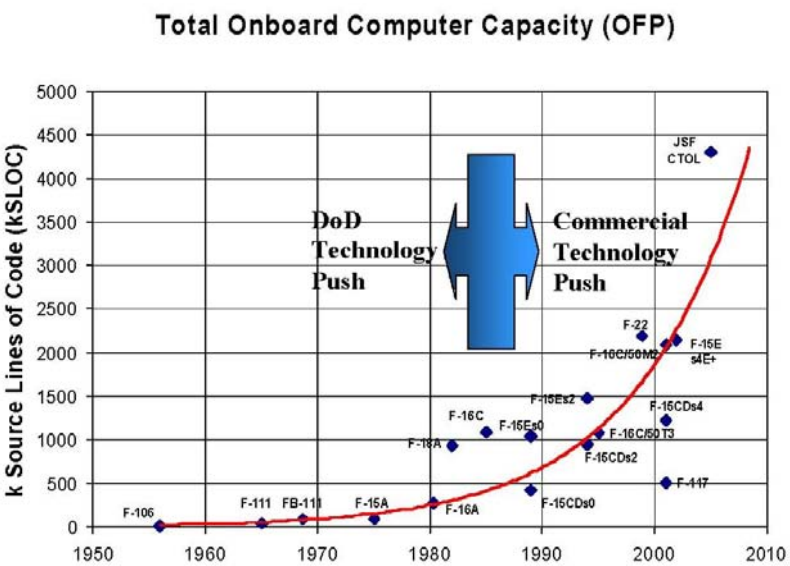
Software Complexity & Cost





- Traditional Embedded SW Development
  - **Low Level Programming**
  - **Ad Hoc Approaches**
  - **Stand-alone, Static Implementations**
  - **Custom Systems**
  - **Little Code Re-use**
  - **V & V is labor intensive (e.g. F/A-22)**
- Result is ….
  - **Prolonged Design Schedules**
  - **Excessive Cost**
  - **Difficulty in Maintenance/ Upgrade/ Retrofit**
  - **Limits on Functionality**
- Looking Ahead
  - **Increased Functionality => Complexity**
  - **Move Towards Networking, Interconnecting Systems**
  - **Distributed Computation Models**
  - **Reconfigurability, Dynamic Modifications**
  - **Code Correctness/ Safety Concerns**
  - **Security**
  - **Shortage of Skilled Programmers**

Advanced tools and techniques are need to address increasing complexity!

Can we preserve historical improvement rates?

Of necessity, innovate in the broader architecture design space

slowing VLSI motivates more architectural exploration

Invest hardware to simplify software

Encapsulate sophisticated software to achieve performance with portability